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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,976	10/28/2003	Amanda Noe	15114-064700US	8004

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EXAMINER

WALTER, CRAIG E

ART UNIT PAPER NUMBER

2188

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/695,976	<b>Applicant(s)</b> NOE, AMANDA	
	<b>Examiner</b> Craig E. Walter	<b>Art Unit</b> 2188	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 September 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 13, 18, 20-21 and 23 is/are rejected.
- 7) ☒ Claim(s) 10-12, 14-17, 19 and 22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***DETAILED ACTION***

***Drawings***

1. The drawings received on 28 October 2003 are deemed acceptable.

***Claim Objections***

2. Claims 2, 9, 10-13 and 15-16 are objected to because of the following informalities:

As for claim 2, the word "circuits" should be changed to "circuit" in line five of the claim. Additionally in line one, the phrase "parallel bit output formats" should be changed to "parallel bit outputs" for clarity. More specifically, a "format" of data cannot be inputted, only the data itself may be inputted into another system (in this instance, a tristate driver circuit).

As for claim 9 (in lines four through five), the phrase "parallel bit output formats" should be changed to "parallel bit outputs" for the same reason as set forth for the objection of claim 2.

As for claims 15-16, the word "position" should be changed to "portion" in line one of these claims.

Claims 10-13 depend on claim 9 therefore they too are objected to. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 3-8, 18, 20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg (US PG Publication 2002/0159483 A1) in further view of Craft (US Patent 5,652,878).

As for claim 1, Clauberg teaches a method comprising:

receiving a serial stream of data bits (paragraph 0023, lines 1-8 – the system can receive unaligned parallel or serial bits);

deserializing the serial stream of data bits into parallel bits (paragraph 0024, lines 1-3 - data is transformed into parallel bits);

inputting the parallel bits into a first register (Fig. 2, the deserializer feeds the parallel data into a register (element 214) via the demux (element 212) – paragraph 0032, lines 1-17);

inputting an output of the first register to a second register (Fig. 2, element 216 – the shift register receives the data from the first register (element 214) – paragraph 0032, lines 1-17);

providing the parallel bits in a plurality of parallel bit output formats (The parallel output from the demux is fed into the shift register (Fig. 2, element 216). The shift register is capable of shifting the outputted data into any of the a

plurality of parallel formats (i.e. the bit at position 1 can be shifted to any of the other 7 positions. Clauberg exploits this shifting pattern in order to align the position of the outputted bits – paragraph 0032, lines 1-17);

Though Clauberg teaches outputting the data from the first two registers (data stored in register (element 214) is sent to the shift register (element 216) which is eventually outputted (element 204)) into a storage unit, (abstract, lines 5-8 – a storage unit stores data from the outgoing data stream), he fails to teach storing the outputted data specifically in a CAM. Further, though it is well known in that art that Clauberg could use any sort of common memory to store his outgoing data (i.e. a RAM), he still fails to teach or suggest specifically using a CAM.

Craft however teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50).

Craft further teaches selecting one of the parallel bit output formats to output based on match flag outputs from the CAM, wherein the match flag outputs are generated in response to the inputs to the CAM (col. 5, lines 1-9 – a plurality of entries are stored in the CAM array, match flag signals (342) are generated based on the comparison of the data stored in the CAM with the data in the input buffer).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to store his outputted parallel data into the CAM as taught by Craft, rather than a standard means, such as with a random access memory. By doing so, Clauberg would benefit by improving the compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57.

As for claim 3, Clauberg teaches the 8 parallel bits (referring paragraph 0024, lines 7-11, the incoming data stream can be either 2, 4, 8, 16 etc. bits. The deserializer would then take the incoming serial bits and convert them to 8, 16, 32, or 64 bits wide respectively as indicated in paragraph 0025, lines 1-5).

As for claim 4, Clauberg teaches the first and second registers as being two stages of a shift register (referring to Fig.2, the two registers (214) and (216) work in tandem to shift the data outputted from the demux hence are two stages of a shift register).

As for claim 5, Craft teaches the depth of the CAM comprising at least one row for each of the parallel bits (col. 6, line 65 through col. 7, line 7 – the CAM array can be 1,012 sections deep. Note Clauberg teaches a taking a 16-bit serial input to generate a 64-bit parallel output in paragraph 0025, lines 1-5).

As for claim 6, Clauberg teaches the inputs of the CAM as being provided by way of parallel transfer (the deserialized data is outputted to storage (i.e. Craft's CAM) via the output port (Fig. 2, element 204)).

As for claim 7, Clauberg teaches the width of the parallel bits input into the CAM as being at least a number of parallel bits output from the deserializer plus a length of a pattern to be detected using the CAM minus 1 (using the example of 64 bits being output from his deserializer (Clauberg, paragraph 0025, lines 1-5 – the output is fed to the CAM via the output (Fig. 2, element 204). The 64 bits are then transmitted to the CAM. These bits are then compared to the word in the input data buffer of the CAM (i.e., the pattern to be detected – Craft, col. 5, lines 1-9). Though the word size is not specifically set forth by Craft, it is well known in the art that a word is 16 bits in length.

As for claim 8, Clauberg teaches a circuit comprising:

a deserializer circuit coupled to receive serial data input and outputting a first parallel data of output (Fig. 2, element 206 – paragraph 0031, lines 1-2); and

a shift register coupled to the first parallel data output (Fig. 2, element 216 – paragraph 32, lines 1-9);

Though Clauberg teaches storing the outputted parallel data (abstract, lines 5-8 – a storage unit stores data from the outgoing data stream), he fails to teach storing the outputted data specifically in a CAM. Further, though it is well known in that art that Clauberg could use any sort of common memory to store his outgoing data (i.e. a RAM), he still fails to teach or suggest specifically using a CAM, hence failing to meet all of the limitations of claim 8.

Craft however teaches a method and apparatus of compressing data, which includes a circuit for storing incoming data (col. 2, lines 59-63). More specifically, Craft teaches implementing his circuit by use of a CAM rather than a RAM (col. 3, lines 42-50).

As for claim 18, Craft teaches the circuit of claim 8 wherein the CAM has a number of rows equal to or greater than a number of bits of the first parallel data output (col. 6, line 65 through col. 7, line 7 – the CAM array can be 1,012 sections deep. Note Clauberg teaches a taking a 16-bit serial input to generate a 64-bit parallel output in paragraph 0025, lines 1-5).

As for claim 20, Clauberg teaches the circuit of claim 8 wherein the first parallel data output is 8, 16, or 32, etc. bits wide (referring paragraph 0024, lines 7-11, the incoming data stream can be either 2, 4, 8, 16 etc. bits. The deserializer would then take the incoming serial bits and convert them to 8, 16, 32, or 64 bits wide respectively as indicated in paragraph 0025, lines 1-5).

As for claim 23, Clauberg teaches the circuit of claim 8, wherein the first parallel data output comprises 8 bits (again referring to paragraph 0024, lines 7-11, the incoming data stream can be 2 bits, producing a 8-bit parallel output via the 1:4 demultiplexer). The parallel output from the demux is then fed into the shift register (Fig. 2, element 216). The shift register is capable of shifting the outputted data into any of the eight claimed formats (i.e. the bit at position 1 can be shifted to any of the other 7 positions. Likewise each of corresponding remaining seven bits would shift relative to the first. Clauberg exploits this



shifting pattern in order to align the position of the outputted bits – paragraph 0032, lines 1-17).

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to store his outputted parallel data into the CAM as taught by Craft, rather than a standard means, such as with a random access memory. By doing so, Clauberg would benefit by improving the compressing ratio of the stored data, and increase throughput during transmission of the data as taught by Craft in col. 3, lines 50-57.

4. Claims 2, 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg and Craft as applied to claims 1 and 8 above, and in further view of Morikawa (US Patent 6,7470,886).

As for claim 2, though the combined teachings of Clauberg and Craft fail to teach outputting the parallel bit outputs into a plurality of tristate driver circuits, Morikawa teaches a content addressable memory with shifted enable signal which includes an input-output circuit which includes tristate buffers (ND1, ND2) – col. 3, lines 43-54. In his disclosure, Morikawa teaches inputting data outputted from cells the CAM (Fig. 3, element 2) into the input-output circuit (Fig. 3, element 10), which is comprised of a plurality of tristate buffer drivers circuits. Data is the selected via the input-output circuit and outputted as the data output signal DOUT – col. 3, lines 43-54). This selection occurs based on the RWN control signal which enables ND2 to output the signal.

As for claim 9, though the combined teachings of Clauberg and Craft teach a plurality of parallel data output formats based on the first parallel data output, they fail

coupling a plurality of tristate buffer circuits to each of the parallel data outputs.

Morikawa however teaches a content addressable memory with shifted enable signal, which includes an input-output circuit, including tristate buffers (ND1, ND2) – col. 3, lines 43-54. In his disclosure, Morikawa teaches inputting data outputted from cells the CAM (Fig. 3, element 2) into the input-output circuit (Fig. 3, element 10), which is comprised of a plurality of tristate buffer drivers circuits.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg to include Morikawa's CAM with shifted enable signal to his system byte alignment unit. By doing so, Clauberg would benefit from Morikawa's shifting in logic level of the enable signal of his memory which in turn would help to reduce the current consumption of the memory cell, and speed up read/write access of the memory as taught by Morikawa in col. lines 8-13.

As for claim 13, Clauberg teaches one parallel data output format for each bit of the first parallel data output minus 1 (assuming the first parallel output consists of 8 bits (i.e. 2 bit input to the 1:4 demux – paragraph 0024, lines 7-11), Clauberg teaches at least seven more possible parallel data outputs (i.e. 16, 32, 64, ..., 1024 bits).

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Clauberg and Craft as applied to claim 8 above, and in further view of Veenstra et al., hereinafter Veenstra (US Patent 6,160,419).

Though the combined teachings of Clauberg and Craft include a circuit including a CAM, a shift register, and a deserializer as claimed by Applicant in

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claim 8, they fail to disclose making use the circuit in a programmable logic IC implementation as claimed by Applicant.

Veenstra however teaches a programmable logic architecture incorporating a content addressable embedded array block. In his disclosure, Veenstra teaches a programmable IC which is configured to operate as CAM (col. 2, lines 52-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Clauberg in further view of Craft to implement his byte alignment unit on the field programmable logic device as taught by Veenstra. By doing so, Clauberg would be able to exploit the benefits of post-manufacturing customization of the circuit as taught by Veenstra in col. 1, lines 26-43).

***Allowable Subject Matter***

6. <sup>10-12/</sup>Claims 14, 17, 19 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter:

As for claim 10, neither Craft, nor Clauberg, nor Morikawa teach a control logic block, coupled to a match signal from the CAM, generating a plurality of

select signals, coupled to each of the tristate buffer circuits as claimed by applicant.

As for claim 14, though Clauberg teaches coupling a shift register to the deserializer circuit, he fails to further teach the register as comprising three portions, of which one is coupled to the deserializer circuit through a mux, the second portion connected to the first mux and a third connected to the second portion via a second mux as claimed by Applicant.

As for claim 17, Clauberg in further view of Craft fail to each row in the CAM comprising a data pattern to be detected in the serial data input.

As for claim 19, Clauberg in further view of Craft fails to teach the CAM comprising a bit pattern comprising "1111", "0110", "0010", 1000" in at least a number of rows that is equal to a number of bits of the first parallel data output.

As for claim 22, Clauberg teaches producing a plurality of parallel data outputs based on the first parallel data out by use of the shift register. Further, though Clauberg teaches a selector circuit for outputting one of the parallel data output formats (Fig. 2, element 222 – paragraph 0032, lines 11-17 – the extractor extracts the 64-bit parallel bit pattern), he fails to teach a selecting one of the outputs based on an output from the CAM as claimed by Applicant.

Claims 11-12 further limit claim 10, therefore are deemed allowable.

Claims 15-16 are believed to be allowable over the prior art of record, however they must be rewritten to overcome the objection set forth under section two of this correspondence.

**Conclusion**

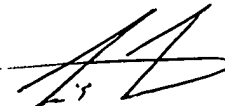
8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Pereira (US Patent 6,490,650 B1) teaches a method and apparatus for generating a device index in a CAM.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Craig E Walter  
Examiner  
Art Unit 2188

CEW

  
MANO PADMANABHAN  
SUPERVISORY PATENT EXAMINER